

ABSTRACT OF THE DISCLOSURE

A sharing mechanism is herein disclosed for multiple logical processors using a translation lookaside buffer (TLB) to translate virtual addresses, for example into physical addresses. The mechanism supports sharing of TLB entries among logical processors, which may access address spaces in common. The mechanism further supports private TLB entries among logical processors, which for example, may each access a different physical address through identical virtual addresses. The sharing mechanism provides for installation and updating of TLB entries as private entries or as shared entries transparently, without requiring special operating system support or modifications. Through use of the disclosed sharing mechanism, fast and efficient virtual address translation is provided without requiring more expensive functional redundancy.